REMARKS

By the present amendment, claims 1 and 14 have been amended. Reconsideration and allowance of outstanding claims 1-23 in view of the above amendments and following remarks are requested.

A. Rejection of Claims 1-23 under 35 USC §103(a)

The Examiner has rejected claims 1-23 under 35 USC §103(a) as being obvious with respect to U.S. Patent Number 5,640,048 to Selna ("Selna") and U.S. Patent Number 5,942,797 to Terasawa ("Terasawa"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 14, is patentably distinguishable over Selna and Terasawa.

Various embodiments according to the present invention, as defined by independent claim 1, teach a structure including vias providing connections between a plurality of semiconductor dies and first and second heat spreaders. Various embodiments according to the present invention, as defined by independent claim 1, teach a structure including vias providing connections between a plurality of semiconductor dies and a single heat spreader.

One advantage of the single heat spreader structure, as disclosed in the present application on page 44, is that single heat spreader 967 effectively acts as two heat spreaders in parallel. The single heat spreader structure 900 further reduces inductive and resistive paths from the ground of PCB 998 to support pads 917 and 919. The reduction

in inductive and resistive paths results in less noisy grounds for semiconductor dies 910 and 912 and further ensures that the ground voltage levels of semiconductor dies 910 and 912 do not rise to far above, or fall too far below zero volts.

A further advantage achieved by the single heat spreader structure 900 is that the single heat spreader 967 achieves further structural stability since its continuous structure results in a further reduction of strain on the solder joints connecting PCB 998 to structure 900. The single heat spreader structure 900 also results in more efficient heat conduction.

Referring to the present application at page 45, one advantage of the two separate heat spreaders 859 and 861 in structure 800, as defined by independent claim 1, is the fact that the two semiconductor dies 810 and 812 and their respective support pads 817 and 819 and heat spreaders 859 and 861 need not be in close proximity to each other. Thus, structure 800 achieves increased flexibility in the locations of semiconductor dies 810 and 812 on PCB 898. This flexibility can be advantageous in various circumstances. For example, for ease of wire bonding it may be desired to separate the locations of semiconductor dies 810 and 812 on PCB 898.

Referring to Figure 7 and page 45 of the present application, a still further advantage is realized, common to the structures defined by both independent claim 1 and independent claim 14. Specifically, semiconductor die signal bond pads on two semiconductor dies can be connected not only directly by bonding wires, but also by "traces" on the top surface of the substrate. This technique may achieve a shorter, less resistive and less inductive route than the alternative connection route using vias in

substrate 720, lands on the bottom surface of substrate 720, and traces on the PCB connected to the bottom surface of substrate 720.

Additionally, independent claims 1 and 14 have been amended and recite "wherein said first semiconductor die is coupled both to said second semiconductor die and to said substrate". Support for these amendments appears, for example, in Figure 8 of the present application. Semiconductor die 810 is coupled to semiconductor die 812 via bonding wire 846. Semiconductor die 810 is coupled to the substrate by bonding wire 816.

Advantageously, due to the configuration as defined by amended independent claims 1 and 14, the length of bonding wires coupling the first semiconductor die to the substrate and to the second semiconductor die can be minimized. Thus, structure 800 provides low resistance, low inductance, and minimal length of electrical connections. Parasitic inductance and resistance can also be advantageously decreased.

In contrast to the present invention as defined by amended independent claims 1 and 14, Selna merely discloses IC 12, printed circuit board material 52, 54, printed circuit board 18, and conductive and/or thermal vias 6A, 6B, and 6C. The Examiner states, correctly, that Selna does not teach a second chip connected to a heat spreader. Selna also does not disclose, teach, or even suggest that "said first semiconductor die is coupled both to said second semiconductor die and to said substrate." Selna furthermore provides no teaching or suggestion of achieving the advantages inherent in the structure defined by amended independent claims 1 and 14.

Selna does not disclose, teach, or suggest the configuration of amended independent claims 1 and 14, including that the first semiconductor die is coupled both to the second semiconductor die and to the substrate. Furthermore, there is no teaching or suggestion to combine or modify Selna. Therefore, Selna, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claims 1 and 14.

Terasawa does not cure the deficiencies of Selna. Terasawa is directed to a power semiconductor module in which a plurality of power semiconductor elements forming a bridge circuit are provided together with control circuits. Terasawa teaches two semiconductor elements 1. However, semiconductor elements 1 are not even coupled to vias. Terasawa also does not disclose, teach, or even suggest that "said first semiconductor die is coupled both to said second semiconductor die and to said substrate." Terasawa furthermore provides no teaching or suggestion of achieving the advantages inherent in the structure defined by independent claims 1 and 14. Further, there is no teaching or suggestion to combine or modify Selna and Terasawa to achieve the non-obvious structure and advantages of the present invention discussed herein. Selna and Terasawa, singly or in combination, do not teach, disclose, or even suggest the advantageous structure defined by amended independent claims 1 and 14.

Terasawa does not disclose, teach, or suggest the configuration of amended independent claims 1 and 14, including that the first semiconductor die is coupled both to the second semiconductor die and to the substrate. Furthermore, there is no teaching or

suggestion to combine or modify Terasawa. Therefore, Terasawa, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claims 1 and 14.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 1 and 14 is not taught, disclosed, or suggested by the art of record. Thus, amended independent claims 1 and 14 are patentably distinguishable over the art of record. As such, the claims depending from amended independent claims 1 and 14 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 14, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-23 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1-23 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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